

PATENT APPLICATION

**LOW ENERGY DOSE MONITORING OF IMPLANTER USING
IMPLANTED WAFERS**

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CROSS-REFERENCES TO RELATED APPLICATIONS

[01] NOT APPLICABLE

STATEMENT AS TO RIGHTS TO INVENTIONS MADE UNDER FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT

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[02] NOT APPLICABLE

REFERENCE TO A "SEQUENCE LISTING," A TABLE, OR A COMPUTER

PROGRAM LISTING APPENDIX SUBMITTED ON A COMPACT DISK.

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[03] NOT APPLICABLE

BACKGROUND OF THE INVENTION

[04] The present invention is directed integrated circuits and their processing for the manufacture of semiconductor devices. More particularly, the invention 20 provides a method for monitoring a low energy dose implantation process for the manufacture of integrated circuits. But it would be recognized that the invention has a much broader range of applicability. For example, the invention can be applied to a variety of devices such as dynamic random access memory devices, static random access memory devices (SRAM), application specific integrated circuit devices (ASIC), microprocessors and 25 microcontrollers, Flash memory devices, and others.

[05] Integrated circuits or "ICs" have evolved from a handful of interconnected devices fabricated on a single chip of silicon to millions of devices. Current ICs provide performance and complexity far beyond what was originally imagined. In order to achieve improvements in complexity and circuit density (i.e., the number of devices 30 capable of being packed onto a given chip area), the size of the smallest device feature, also known as the device "geometry", has become smaller with each generation of ICs.

Semiconductor devices are now being fabricated with features less than a quarter of a micron across.

[06] Increasing circuit density has not only improved the complexity and performance of ICs but has also provided lower cost parts to the consumer. An IC fabrication facility can cost hundreds of millions, or even billions, of dollars. Each fabrication facility will have a certain throughput of wafers, and each wafer will have a certain number of ICs on it. Therefore, by making the individual devices of an IC smaller, more devices may be fabricated on each wafer, thus increasing the output of the fabrication facility. Making devices smaller is very challenging, as each process used in IC fabrication has a limit. That is to say, a given process typically only works down to a certain feature size, and then either the process or the device layout needs to be changed.

[07] An example of a semiconductor process that is important to make smaller and smaller devices is ion implantation for shallow junction MOS devices. Shallow junction MOS devices often require low energies but high impurity doses. Certain types of implantation such as boron use implant energies of 2 keV and possibly less. Such implant energies and doses are often difficult to monitor accurately. Here, measurement of implant depth and other parameters are often difficult or impossible using conventional techniques. In certain conventional techniques, screen oxides are formed on wafers before implantation. Low energy impurities often become trapped in the oxide layer and do not even reach the underlying silicon material. Resistance measurements of such oxide coated waters cannot be made accurately. Alternatively, bare silicon wafers are also implanted with impurities. These wafers often out diffuse the implanted impurities, which cannot be measured to any degree of accuracy. Accordingly, it is difficult to accurately monitor low energy implants for the manufacture of semiconductor devices.

[08] From the above, it is seen that an improved technique for processing semiconductor devices is desired.

BRIEF SUMMARY OF THE INVENTION

[09] According to the present invention, techniques for processing for the manufacture of semiconductor devices are provided. But it would be recognized that the invention has a much broader range of applicability. More particularly, the invention provides a method for monitoring a low energy dose implant process for the manufacture of integrated circuits. For example, the invention can be applied to a variety of devices such as

static random access memory devices (SRAM), application specific integrated circuit devices (ASIC), microprocessors and micro controllers, Flash memory devices, and others.

[10] In a specific embodiment, the invention provides a method for processing semiconductor devices. The method includes providing a monitor wafer, which 5 comprising a silicon material. The method includes introducing a plurality of particles within a depth of the silicon material, whereupon the plurality of particles (e.g., silicon) cause the silicon material to be in an amorphous state. The method also includes introducing a plurality of dopant particles (e.g., boron, arsenic) into a selected depth of the silicon material using an implantation tool. Preferably, the amorphous state traps the dopant particles and may even 10 cause recrystallization of the amorphous silicon material. The method also includes subjecting the monitor wafer including the plurality of particles and dopant particles into thermal anneal process to activate the dopant. The wafer is removed. The method includes measuring a sheet resistivity of a surface region including the implanted dopant particles of the monitor wafer and determining a dose of the dopant bearing impurities. Next, the method 15 includes operating the implantation tool using one or more production wafers if the dose of the dopant particles in the monitor wafer is within a tolerance of a specification limit.

[11] In a specific alternative embodiment, the invention provides a method for processing semiconductor wafers, e.g., silicon. The method includes providing a monitor wafer, which is made of a crystalline material. The method includes introducing a plurality 20 of particles within a depth of the material, whereupon the plurality of particles cause the crystalline material to be in an amorphous state. The method also includes introducing a plurality of dopant particles into a selected depth of the crystalline material in the amorphous state using an implantation tool. The amorphous state traps the dopant particles. The method includes subjecting the monitor wafer including the plurality of particles and dopant particles 25 into thermal anneal process to activate the dopant. The sheet resistivity is measured. The method operates the implantation tool using one or more production wafers if the dose of the dopant particles in the monitor wafer is within a tolerance of a specification limit.

[12] Many benefits are achieved by way of the present invention over 30 conventional techniques. For example, the present technique provides an easy to use process that relies upon conventional technology. In some embodiments, the method provides higher device yields in dies per wafer. Additionally, the method provides a process that is compatible with conventional process technology without substantial modifications to conventional equipment and processes. Preferably, the invention can be applied to a variety of applications such as memory, ASIC, microprocessor, and other devices. Preferably, the

invention provides a way to monitor a low energy dose implantation process for shallow junction devices. Depending upon the embodiment, one or more of these benefits may be achieved. These and other benefits will be described in more throughout the present specification and more particularly below.

5 [13] Various additional objects, features and advantages of the present invention can be more fully appreciated with reference to the detailed description and accompanying drawings that follow.

BRIEF DESCRIPTION OF THE DRAWINGS

10 [14] Figures 1 through 6 are simplified cross-sectional view diagrams illustrating a method according to an embodiment of the present invention;

[15] Figure 4A is a simplified cross-sectional view diagram of a portion of a semiconductor substrate according to an embodiment of the present invention; and

15 [16] Figures 7 through 9 are simplified plots of experimental results according to embodiments of the present invention

DETAILED DESCRIPTION OF THE INVENTION

[17] According to the present invention, techniques for processing for the manufacture of semiconductor devices are provided. But it would be recognized that the invention has a much broader range of applicability. More particularly, the invention provides a method for monitoring a rapid thermal anneal process at low temperatures for the manufacture of integrated circuits. For example, the invention can be applied to a variety of devices such as static random access memory devices (SRAM), application specific integrated circuit devices (ASIC), microprocessors and micro controllers, Flash memory devices, and others.

25 [18] A method for fabricating a monitor substrate for temperature analysis of a low energy dose implantation process according to an embodiment of the present invention is provided as follows:

[19] 1. Provide a monitor wafer, e.g., silicon wafer;

30 [20] 2. Introduce a plurality of particles (e.g., silicon) within a depth of the silicon material to cause an amorphous state within the silicon material;

[21] 3. Introduce boron at low energy and high dose into a depth of the monitor wafer;

[22] 4. Subject the monitor wafer including the plurality of particles and boron into a rapid thermal anneal process at about 700 Degrees Celsius to activate the boron bearing particles;

[23] 5. Remove the monitor wafer;

5 [24] 6. Measure a sheet resistivity of the monitor wafer;

[25] 7. Perform steps 1 through 6 for other monitor wafers having different doses of boron impurities; and

[26] 8. Plot the relationship of sheet resistivity to boron doses; and

[27] 9. Perform other steps, as desired

10 [28] The above sequence of steps is used to prepare a monitor wafer, which will be used to determine an accurate temperature of a rapid thermal anneal process. The monitor wafer is used to make a calibration curve, which will be used to determine a dose of an impurity for another monitor wafer. The calibration curve can be adjusted depending upon the embodiment. Further details of the present method can be found according to the Figures 15 below.

[29] A method for manufacturing an integrated circuit device using an implantation process according to an embodiment of the present invention can be provided as follows:

20 [30] 1. Provide a monitor wafer, e.g., silicon wafer;

[31] 2. Introduce a plurality of particles (e.g., silicon) within a depth of the silicon material to cause an amorphous state within the silicon material;

[32] 3. Introduce boron at low energy and high dose into a depth of the monitor wafer;

25 [33] 4. Subject the monitor wafer including the plurality of particles and boron into a rapid thermal anneal process at about 700 Degrees Celsius to activate the boron bearing particles;

[34] 5. Remove the monitor wafer;

[35] 6. Measure a sheet resistivity of the monitor wafer;

30 [36] 7. Perform steps 1 through 6 for other monitor wafers having different doses of boron impurities; and

[37] 8. Plot the relationship of sheet resistivity to boron doses;

[38] 9. Provide monitor water for production run;

[39] 10. Perform steps 1-6;

[40] 11. Determine dose of impurity based upon plot;

[41] 12. Determine of the dose is within a predetermined tolerance limit for the implantation process;

[42] 13. Perform production operation of product waters using the implantation process if the dose is within the predetermined tolerance;

5 [43] 14. Alternatively, transfer implantation process to maintenance or engineering or calibration;

[44] 15. Perform other steps, as desired

[45] Figures 1 through 6 are simplified cross-sectional view diagrams illustrating a method 100 according to an embodiment of the present invention. These 10 diagrams are merely an illustration, which should not unduly limit the scope of the claims herein. One of ordinary skill in the art would recognize many other variations, modifications, and alternatives. As shown, the method 100 begins by providing a monitor substrate 101, which can be a silicon wafer or the like. Alternative substrates can include any suitable material such as boron and silicon on insulator substrate. Preferably, the monitor wafer is the 15 silicon wafer.

[46] Referring to Figure 2, the method introduces a plurality of particles 105 to cause an amorphous state within a thickness 111 of the monitor substrate. The thickness is defined to a predetermined depth 107, which can be constant or vary slightly, depending upon the application. The particles are introduced through the surface 109 of the 20 substrate using implantation techniques or others. As shown, the particles can be silicon bearing particles such as elemental silicon. Such silicon can be derived from gases such as silane, dichlorosilane, any combination of these, and others. Further details of the amorphous state are described throughout the present specification and more particularly below.

25 [47] Next, the method provides a method of introducing a dopant impurity 305 at low energy and high dose into a depth of the monitor wafer. The dopant impurity can be a boron bearing species, an arsenic bearing species, and others. The energy is often 2 KeV to less than 2 KeV, but can also be at others. The dose is 4×10^{14} to 1×10^{15} atoms/cm², but can also be others. Preferably, the method is used for low energy high dose impurities for 30 shallow junction devices. These devices often have junction depths of less than 40 nm, but can also be at other depths. Additionally, the shallow junction devices are often for line rules of less than 0.15 um. Of course, the particular energies, doses, and depths depend upon the application.

[48] Referring to Figure 4, the implanted profile 400 as a function of depth is illustrated. This profile is merely an example, which should not unduly limit the scope of the claims herein. One of ordinary skill in the art would recognize many alternatives, variations, and modifications. As shown, the vertical axis 401 illustrates concentration. The 5 horizontal axis 403 illustrates depth from the surface of the monitor substrate to the predetermined depth. The profile 405 is substantially even and then reduces in concentration as a function of depth. Further details of such profile are provided below.

[49] Figure 4A is a simplified cross-sectional view diagram of a portion of a semiconductor substrate according to an embodiment of the present invention. This profile 10 is merely an example, which should not unduly limit the scope of the claims herein. One of ordinary skill in the art would recognize many alternatives, variations, and modifications. The portion 450 of the substrate includes silicon bearing species and boron bearing species. Some of the silicon bearing species is from the original substrate material. Other silicon bearing species have been implanted. Such silicon bearing species have broken bonds 451 15 and form an amorphous state within the substrate. The substrate is substantially free from an overlying oxide layer, which may interfere with the boron implantation. There may be a very small layer of oxide, but is substantially ineffective as a screen oxide or other like material. Boron bearing species 453 are also included. Such boron bearing species have not been activated in part according to a specific embodiment. Accordingly, the monitor substrate 20 including the implanted species should be subjected to a thermal process, such as rapid thermal anneal.

[50] Here, the method subjects the monitor wafer including the plurality of particles and boron into a rapid thermal anneal process at about 700 Degrees Celsius to activate the boron bearing particles. Depending upon the embodiment, other temperatures 25 can be used. For example, the temperature can range from about 650 Degrees Celsius to about 700 Degrees Celsius. The rapid thermal anneal process also recrystallizes certain portions of the silicon material. The monitor wafer is then removed and ready for subsequent processing.

[51] The method measures a sheet resistivity of the monitor wafer. The 30 sheet resistivity can be measured using a probe and tool such as KLA Tencor Rs-75, but can also be others. The sheet resistivity is kept for further analysis. The method then performs the above steps for other monitor wafers having different doses of boron impurities. The doses have also been provided with a tool that has been calibrated according to a preferred embodiment.

[52] Referring to Figure 5, the method plots the relationship of sheet resistivity to boron doses according to a specific embodiment. As shown, the monitor wafers include different respective doses, which have been plotted against sheet resistivities. Here, the plot provides a standard to be used in performing, for example, process checks on a specific tool being monitored. The horizontal axis represents sheet resistivity values, and the vertical axis represents doses. As shown, the sheet resistivity increases with lower doses as a general trend. Depending upon the embodiment, any of the above steps may be modified. Alternative processes may be included. The order of the specific steps may also be altered without departing from the scope of the claims herein. One of ordinary skill in the art would recognize many other variations, modifications, and alternatives.

[53] Although the above has been illustrated according to a specific embodiment, there can be other modifications, alternatives, and variations. For example, boron has been used as an impurity, but other impurities such as arsenic and phosphorus can also be used. Additionally, a third implant can also be used to form the monitor substrate. Further, additional ways of causing the amorphous state can also be used. It is also understood that the examples and embodiments described herein are for illustrative purposes only and that various modifications or changes in light thereof will be suggested to persons skilled in the art and are to be included within the spirit and purview of this application and scope of the appended claims.

[54] In a specific embodiment, the invention also provides a method for manufacturing an integrated circuit device using an implantation process according to an embodiment of the present invention. Here, the method can be used to check the process of a specific implantation tool. The method is often performed during a predetermined frequency or other desirable times for the specific implantation tool. As shown in Figure 6, the method begins at start, step 601. The method is performed for checking a specific implantation tool, step 603. Before production operation, the monitor wafer is (step 605) inserted into the implantation tool, which would be evaluated.

[55] The method introduce a plurality of particles (e.g., silicon) within a depth of the silicon material to cause an amorphous state within the silicon material. The method then introduce boron at a selected low energy and selected high dose into a depth of the monitor wafer. The dopant impurity can be a boron bearing species, an arsenic bearing species, and others. The energy is often 2 KeV to less than 2 KeV, but can also be at others. The dose is 4×10^{14} to 1×10^{15} atoms/cm², but can also be others. Preferably, the method is used for low energy high dose impurities for shallow junction devices. These devices often

have junction depths of less than 40 nm, but can also be at other depths. Additionally, the shallow junction devices are often for line rules of less than 0.15 um. Preferably, the dose and energy are pre-selected but are provided for process checking before the production run of wafers. Of course, the particular energies, doses, and depths depend upon the application.

5 [56] The method then subject the monitor wafer including the plurality of particles and boron into a rapid thermal anneal process at about 700 Degrees Celsius to activate the boron bearing particles. Depending upon the embodiment, other temperatures can be used. For example, the temperature can range from about 650 Degrees Celsius to about 700 Degrees Celsius. The rapid thermal anneal process also recrystallizes certain 10 portions of the silicon material. Preferably, the temperature is pre-selected for the process check. The monitor wafer is then removed and ready for subsequent processing.

15 [57] The method measures a sheet resistivity of the monitor wafer. The sheet resistivity can be measured using a probe and tool such as KLA Tencor Rs-75, but can also be others. The method then determines (step 607) a dose of impurity based upon plot, which had been previously explained. The method determines (step 608) of the dose is within a predetermined tolerance limit for the implantation process. The predetermined tolerance is often the specification limit for the particular implantation tool and process. If the tool is in specification, the method releases the tool to run production waters, step 609. 20 Alternatively, the method turns the tool over to a maintenance and/or calibration process, step 613. Preferably, the method runs production for at least 24 hours until another monitor water is checked to ensure the quality of the process. The method stops at step 611.

25 [58] Although the above has been illustrated according to a specific embodiment, there can be other modifications, alternatives, and variations. For example, boron has been used as an impurity, but other impurities such as arsenic and phosphorus can also be used. Additionally, a third implant can also be used to form the monitor substrate. Further, additional ways of causing the amorphous state can also be used. It is also understood that the examples and embodiments described herein are for illustrative purposes only and that various modifications or changes in light thereof will be suggested to persons skilled in the art and are to be included within the spirit and purview of this application and 30 scope of the appended claims.

[59] Experiments:

[60] To prove the principle and operation of the present invention, we performed experiments. These experiments are merely examples, which should not unduly

limit the scope of the claims herein. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. Further details of such experiments are provided throughout the present specification and more particularly according to the figures below.

[61] We performed these experiments using conventional tools and a desire 5 to discover improved processes for semiconductor integrated circuits. continued device scaling often required a formation of ever-shallower, low-resistance junctions. The use of ultra-low energy implant and spike anneals made it possible to develop sub-micron technology. A combination of ultra-low energy implant and spike anneals are often desirable to form ultra shallow junctions. The implantation energy can be lowered to sub KeV level. It 10 is often necessary to monitor low energy implantation performance. Annealing is a big issue for low energy implantation monitor, out-diffusion happens when annealing without O₂ or screen oxide, resulting in worse uniformity; annealing with O₂ or screen oxide will often impact dosage accuracy. Here, silicon implantation was used to get amorphous silicon before boron implantation. The wafer can be annealed at lower temperature without O₂ or screen 15 oxide.

[62] Referring to Figure 7, we plotted Rs-to-dose sensitivity testing results. The implantation conditions included silicon/20KeV/1 x 10¹⁵ atoms/cm² before boron/2KeV/4 x 10¹⁴ atoms/cm². Annealing conditions included 700°C, 30 seconds, N² as annealing ambient. Referring to Figure 8, we have demonstrated the dependence of Rs changes upon 20 annealing temperature. Here, implantation conditions included silicon/20KeV/1 x 10¹⁵ atoms/cm² before boron/2KeV/4 x 10¹⁴ atoms/cm² and annealing conditions used were from 650 to 700°C, 30 seconds, N² as annealing ambient.

[63] We have provided our results in Table 1 of Figure 9, which shows the effect of silicon implantation on boron activation. Here, implantation conditions included 25 silicon/20KeV/1 x 10¹⁵ atoms/cm² before boron/2KeV/4 x 10¹⁴ atoms/cm² and annealing conditions were 700°C, 30 seconds, N₂ as annealing ambient. As shown in Table 1, implantation with boron only shows very high sheet resistance. Boron implanted into the wafer was not activated. Silicon implantation before Boron implantation can be helpful for boron activation, Rs of 442.7 ohms/cm² was obtained (uniformity: 0.33%).

[64] As has been demonstrated, pre-amorphous silicon implantation can be 30 benefit for Boron activation. No oxygen or screen oxide was needed for annealing, that will be good to monitor low energy implanter. The sensitivity of 0.83% (Δ Rs/ Δ Dose) was

obtained in the present study. Of course, one of ordinary skill the art would recognize many variations, alternatives, and modifications.

[65] It is also understood that the examples and embodiments described herein are for illustrative purposes only and that various modifications or changes in light 5 thereof will be suggested to persons skilled in the art and are to be included within the spirit and purview of this application and scope of the appended claims.